REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1-25 are now present in this application. Claims 1, 15 and 22 are independent.

Claims 1, 3, 11, 15, 17 and 22 have been amended. Reconsideration of this application, as amended, is respectfully requested.

Priority Under 35 U.S.C. § 119

Applicants thank the Examiner for acknowledging Applicants' claim for foreign priority under 35 U.S.C. § 119, and receipt of the certified priority document.

Drawings

Applicants acknowledge receipt of the Notice of Draftsperson's Patent Drawing Review Form PTO-948 indicating that the formal drawings have been objected to by the Draftsperson. Corrected formal drawings will be filed upon allowance of the instant application.

Rejection Under 35 U.S.C. § 112, 2nd Paragraph

Claim 22 stands rejected under 35 U.S.C. § 112, 2nd Paragraph. This rejection is respectfully traversed.

The Examiner rejected claim 22 because the recitation "forming an insulating layer electrically insulating said gate line and gate electrode" is in contradiction with the limitation "forming a gate line and gate electrode connected thereto on a transparent substrate".

In order to overcome this rejection, Applicants have amended claim 22 to recite forming an insulating layer *over* said gate line and gate electrode. Applicants respectfully submit that the claims, as amended, particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 1-4, 6-8, 10-19, and 21-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,172,728 to Hiraishi. This rejection is respectfully traversed.

Hiraishi discloses a pixel electrode 4 disposed above a thin film transistor (TFT) having a gate electrode 12, said pixel electrode 4 serving as a light shielding layer for the TFT and gate electrode (see FIGS. 2, 6 and 9). With regard to the structure shown in FIG.4, a pixel electrode is not provided as a light-shielding layer, but light-shielding layer 23 is provided instead, to cover the gate electrode

12 for the purpose of shielding light therefrom. For a discussion of the light shielding pixel electrode and layer, see Col.7, lines 7-10 and Col.9, lines 12-14.

The Examiner asserts that Hiraishi provides a low-reflective film on the source line. However, the device of Hiraishi still provides a light shielding means (pixel electrode 4 and light-shielding layer 23) for both the gate and data line in spite of the low-reflective layer. Hence, the low-reflective layer of Hiraishi provides no hint or suggestion to substitute the low-reflective layer for the light shielding layers already used in the device shown.

Further, Hiraishi does not disclose or suggest other recited features of Applicants' claims (as amended). Particularly, Hiraishi does not disclose or suggest a pixel electrode formed on the surface of the passivation layer, but not over said gate electrode to act as a light shielding layer therefor, said pixel electrode providing a gap space over said data line so as not to shield light therefrom, as recited in independent claim 1 (as amended), and similarly stated in independent claims 15 and 22 (as amended).

Claims 2-4, 6-8, 10-14, 16-19, 21 and 23-25 depend, either directly or indirectly on independent claims 1, 15 and 22. Since Hiraishi does not disclose or suggest the features of independent claims 1, 15 and 22, Hiraishi cannot render claims 2-4, 6-8, 10-14, 16-19, 21 and 23-25 obvious to one of ordinary skill in the art. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Claims 5, 9 and 20 stand rejected under 35 U.S.C. 103(a) over Hiraishi in view of Applicants' Related Art (Applicants have not admitted Prior Art). This rejection is respectfully traversed.

Applicants respectfully submit that claims 5, 9 and 20 depend, either directly or indirectly on independent claims 1 and 15 (argued above). Hiraishi does not disclose or suggest the features of independent claims 1 and 15. Therefore, Hiraishi, alone, cannot render claims 5, 9 and 20 obvious to one of ordinary skill in the art. Moreover, Applicants' discuss of related art fails to cure the deficiencies of Hiraishi, discussed above.

Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone

Percy L. Square, Registration No. 51,084, at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

1. (Amended) A liquid crystal display (LCD), comprising:

a gate line formed on a transparent substrate, said gate line having a gate electrode connected thereto;

a data line crossing said gate line and formed on said transparent substrate;

an insulating layer electrically insulating said data line from said gate line;

a thin film transistor formed at an intersection of said gate line and said data line, and connected to said gate line and said data line; [and]

a passivation layer formed over the thin film transistor;

a pixel electrode formed on the surface of the passivation layer, but not over said gate electrode to act as a light shielding layer therefor, said pixel electrode providing a gap space over said data line so as not to shield light therefrom; and

a low reflective layer formed on at least a portion of said data line, said data line having no light shielding layer formed thereover.

3. (Amended) The LCD of claim 2, wherein said [thin film transistor includes connected to said gate line; and a gate electrode said] low reflective layer is formed on said gate electrode.

11. (Amended) The LCD of claim 1, [further comprising:

a] wherein said passivation layer is formed over said gate line, said data line[, said thin film transistor] and said low reflective layer[;] and

[a] said pixel electrode formed on said passivation layer is [and] connected via a contact hole in said passivation layer to said thin film transistor.

15. (Amended) A method of manufacturing a liquid crystal display, comprising:

forming a gate line and a portion protruding from said gate line to serve as a gate electrode of a thin film transistor on a transparent substrate;

forming an insulating layer electrically insulating said gate line;

forming a data line over said transparent substrate and crossing said gate line; [and]

forming a passivation layer over the thin film transistor;

forming a pixel electrode on the surface of the passivation layer, but not over said gate electrode to act as a light shielding layer therefor, said pixel electrode providing a gap space over said data line so as not to shield light therefrom; and

first forming a low reflective layer over at least a portion of said data line, said data line having no light shielding layer formed thereover.

17. (Amended) The method of claim 16, wherein [said forming a gate line step forms a portion protruding from said gate line to serve as a gate electrode of a thin film transistor; and]

said second forming step forms said low reflective layer over said gate electrode.

22. (Amended) A method of manufacturing a liquid crystal display, comprising:

forming a gate line and gate electrode connected thereto on a transparent substrate;

forming an insulating layer over [electrically insulating] said gate line and gate electrode;

forming a semiconductor layer over said gate electrode;

forming a data line crossing said gate line, a source electrode connected to said data line and on a first portion of said semiconductor layer, and a drain electrode on second portion of said semiconductor layer;

forming a low reflective layer over at least a portion of said data line, said data line having no light shielding layer formed thereover;

forming a passivation layer having a contact hole exposing said drain electrode over said transparent substrate; and

forming a pixel electrode on said passivation layer but not over said gate electrode to act as a light shielding layer therefor, said pixel electrode providing a gap space over said data line so as not to shield light therefrom and connected to said drain electrode via said contact hole.